FIG.1

FIG.2

FIG.3A

FIG.3B

FIG.4A

FIG.4B

FIG.5

FIG.6

FIG.7

FIG.8

MEMORY ARRAY 1

FIG.9

FIG.10A

EVEN PAGE (DEFECTIVE COLUMN ADDRESS)
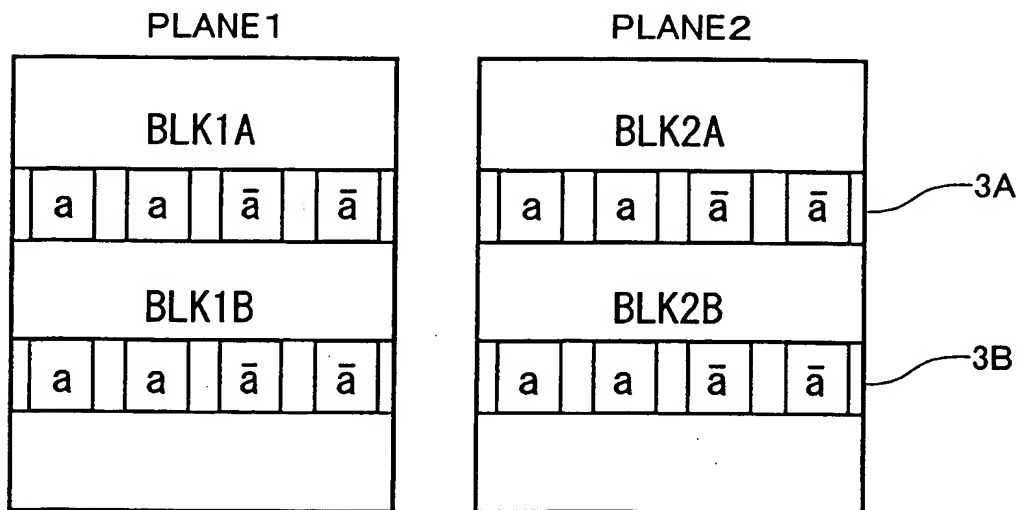
FIG.10B

ODD PAGE (DEFECTIVE BLOCK ADDRESS+OPTION DATA)

FIG.11

POWER-ON OR COMMAND LOAD
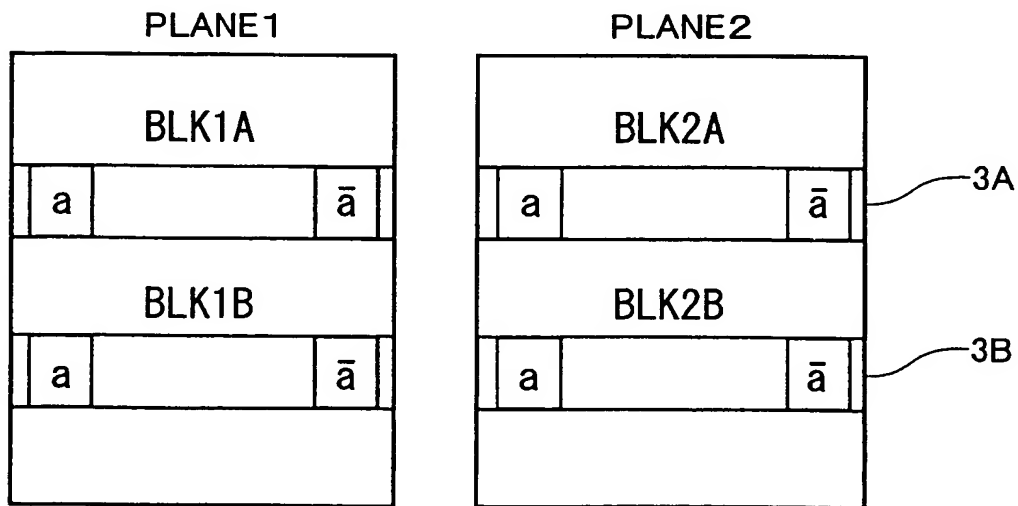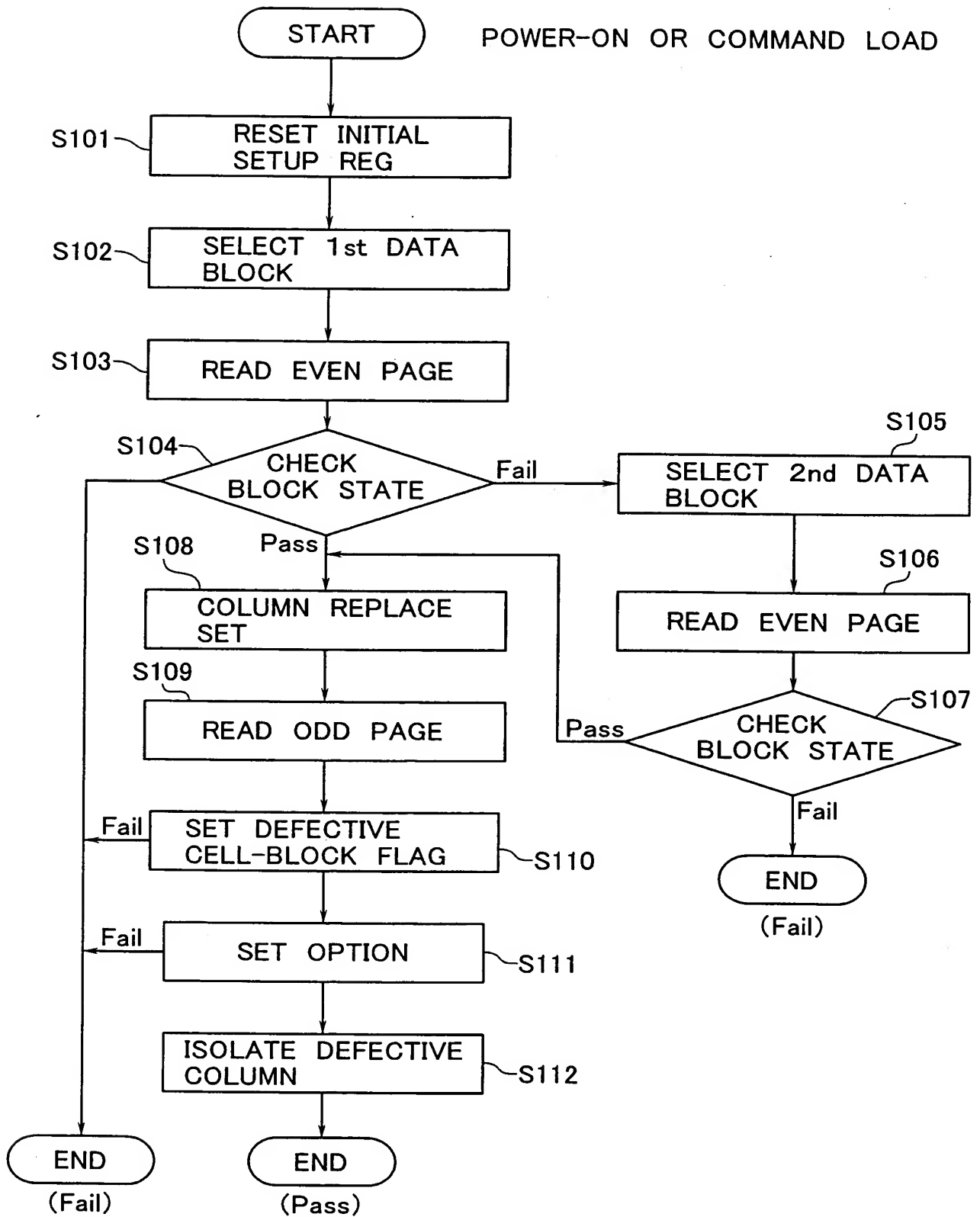
FIG.12
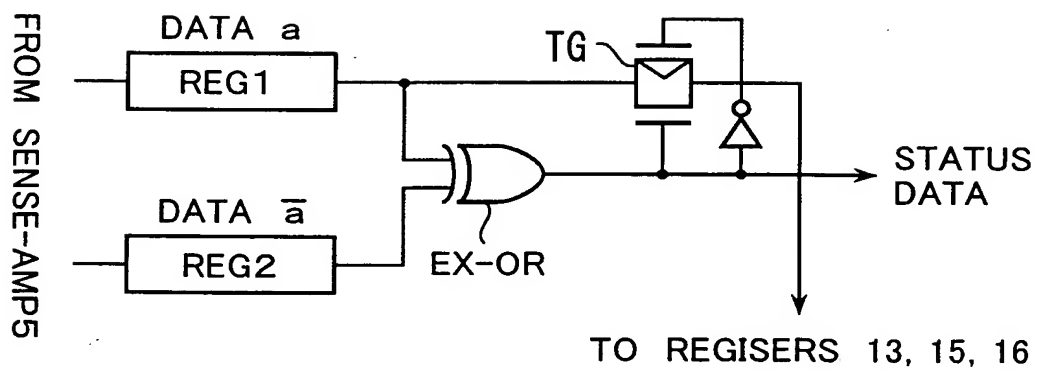
FIG.13

BLOCK STATE CHECH AT S104 & S107

k: NORMAL DATA #
i: COLUMN ADDRESS
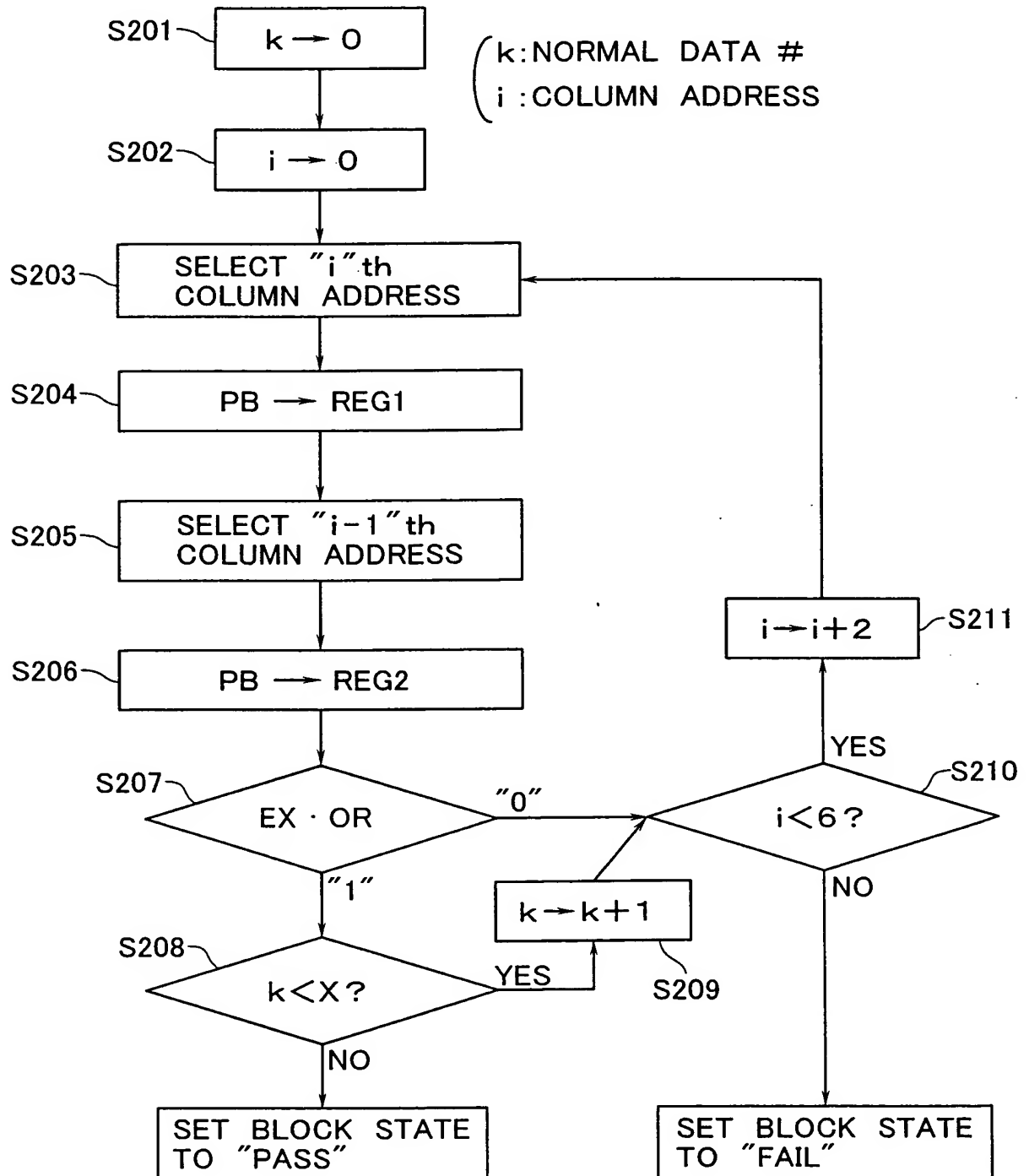
FIG.14

COLUMN REPLACE／SETTING AT S108

k : NORMAL DATA #
i : COLUMN ADDRESS
j : COLUMN REPLACE #

S301 — j → 0

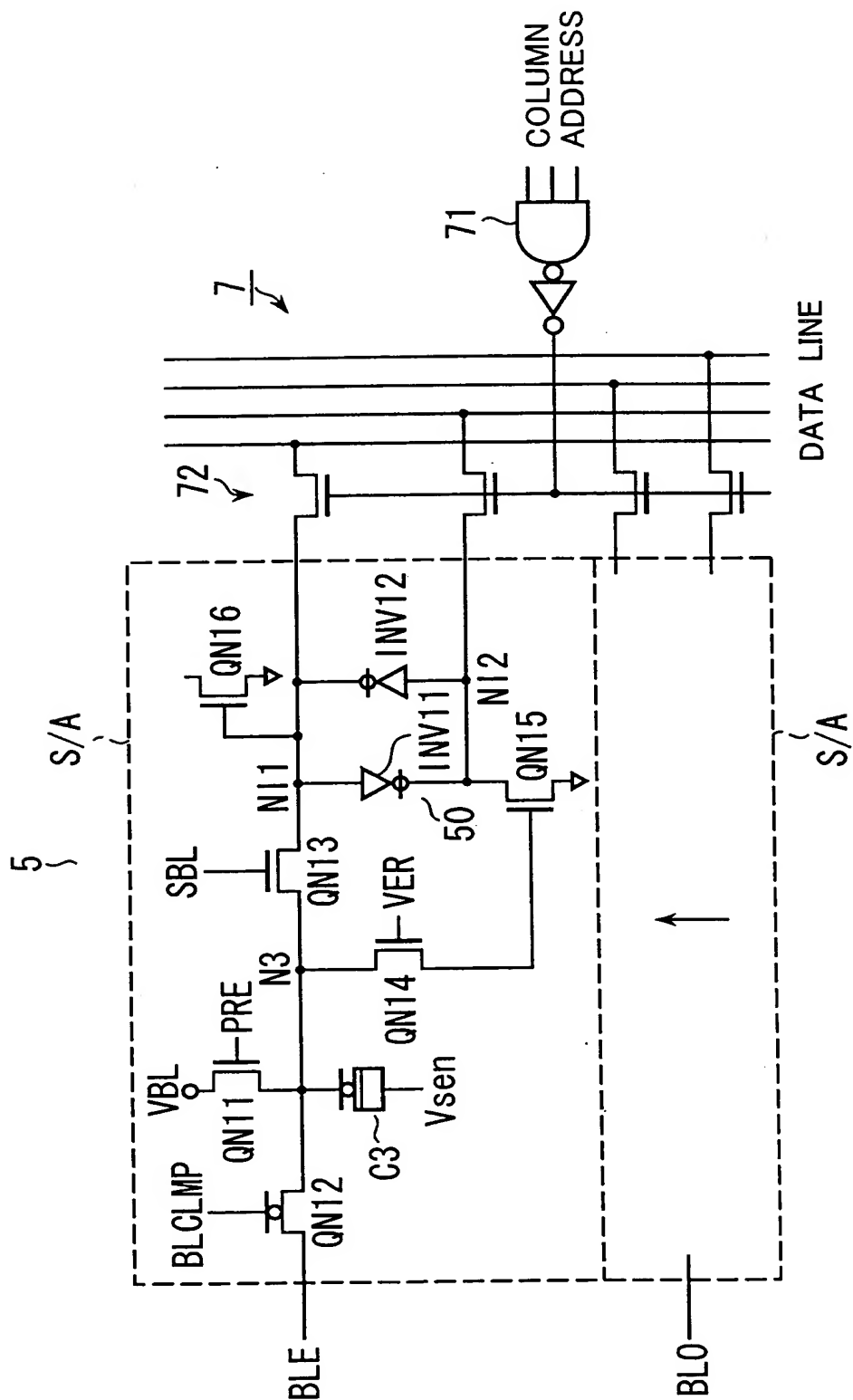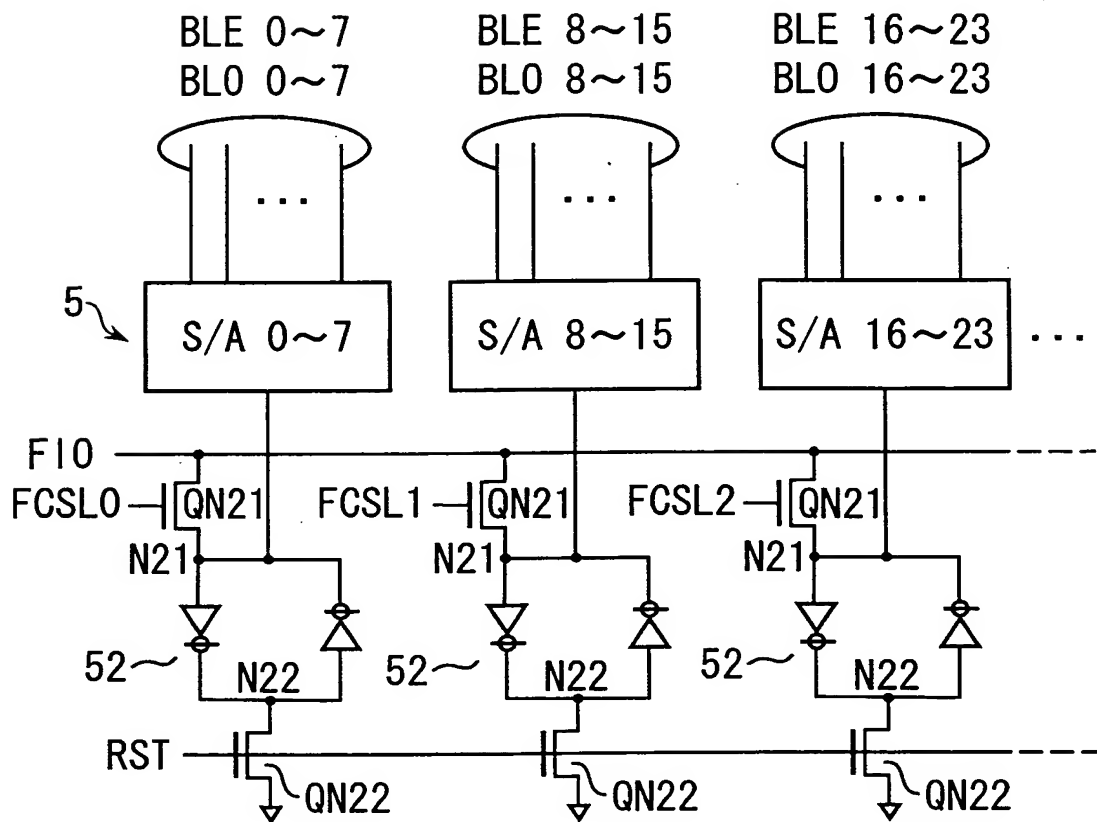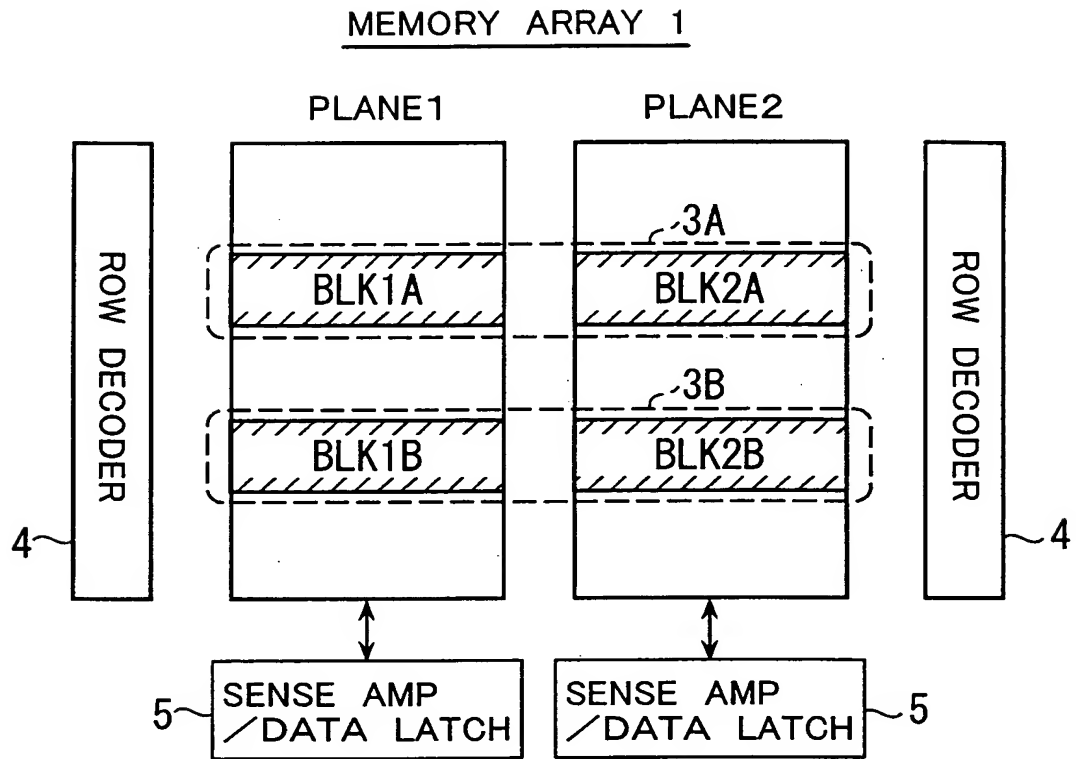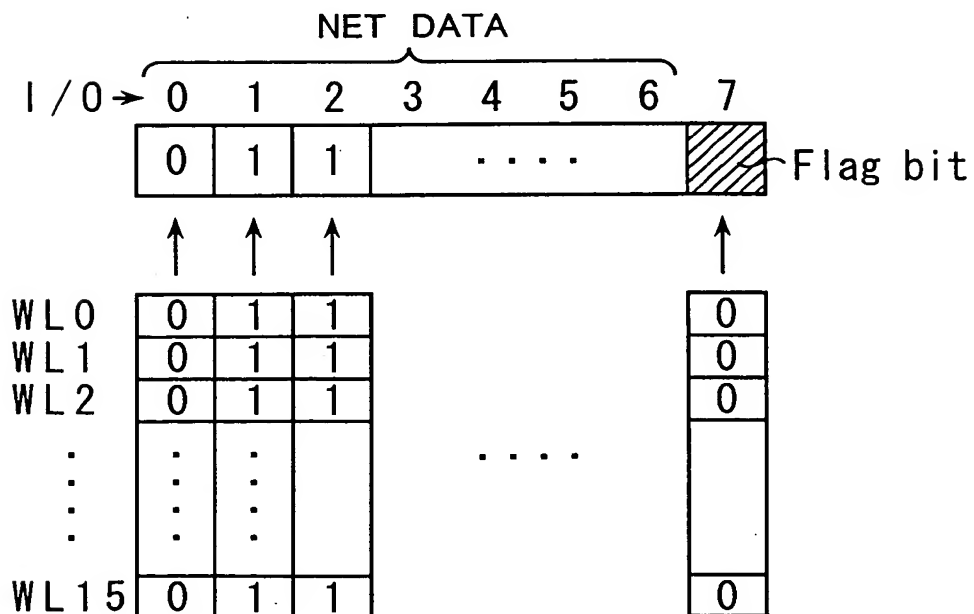S302 — k → 0

S303 — i → 0

SELECT j／i—th COLUMN ADDRESS — S304

PB → REG1 — S305

SELECT j／(i+1) th COLUMN ADDRESS — S306

S312 — i → i+2

PB → REG2 — S307

S315 — j → j+1

S311 — i<6 ? — YES / NO

S308 — EX · OR — "0" / "1"

S314 — j<31 ? — YES / NO

k → k+1 — S310

S309 — k<X ? — YES / NO

S316 — MAKE SENSE-AMP INACTIVE

END (Fail)

S313 — REG1 → DEFECTIVE REG

RETURN (Pass)
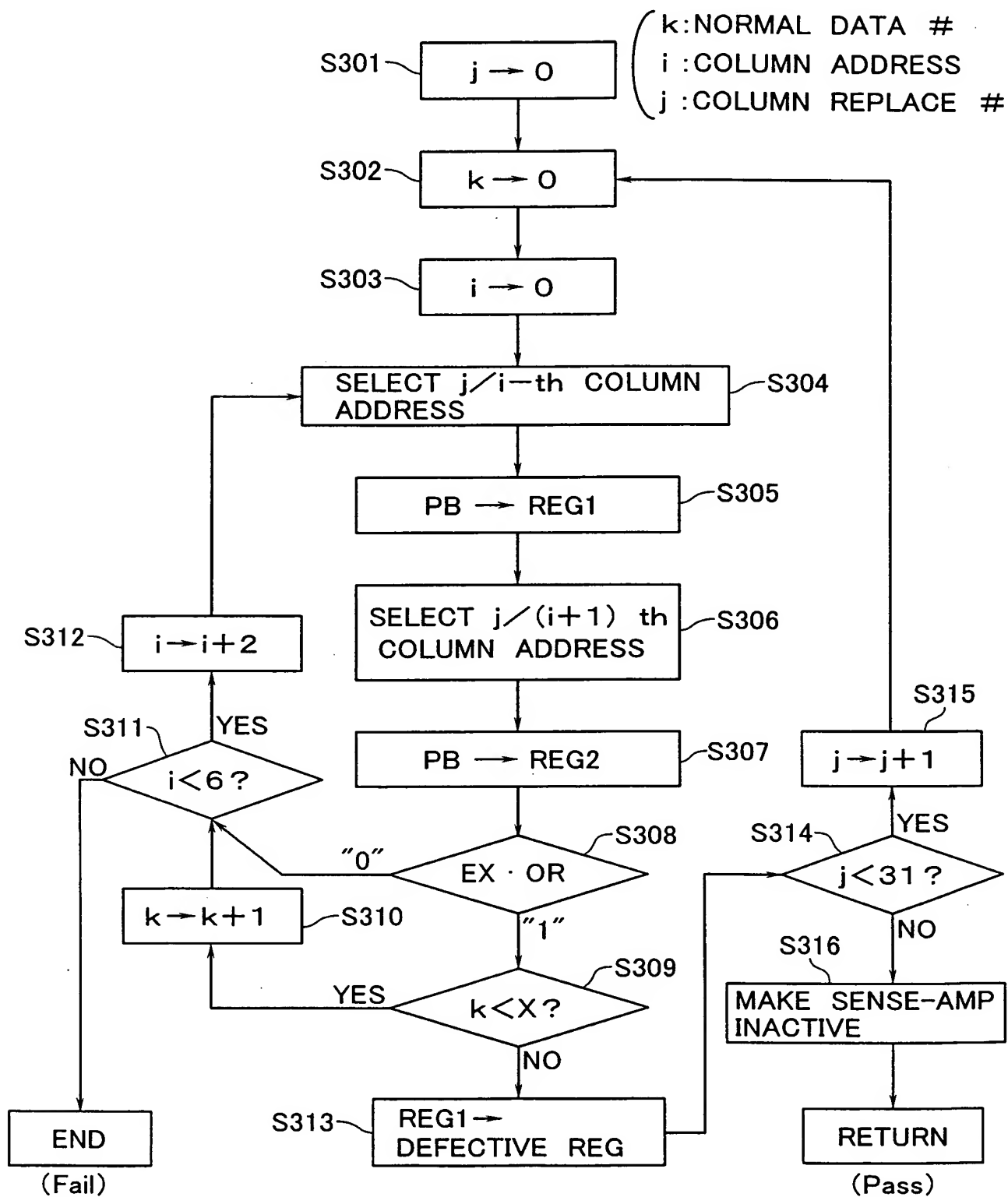
FIG.15

DEFECTIVE CELL-BLOCK
FLAG SETUP AT S110

OPTION SETUP AT S111

(j :DEFECTIVE BLOCK #
  i :COLUMN ADDRESS

S401 — j → 0

S402 — i → 0

S403 — j/i-th COLUMN ADDRESS SELECT

S404 — PB → REG1

S405 — j/(i+1) th COLUMN ADDRESS SELECT

S406 — PB → REG2

S407 — EX-OR

"0" → S409 — i<3?

YES → S410 — i→i+2

NO → END (Fail)

"1" → S408 — Flag="0"?

NO → S412 — j<X?

YES → S413 — j→j+1

NO → RETURN (Pass)
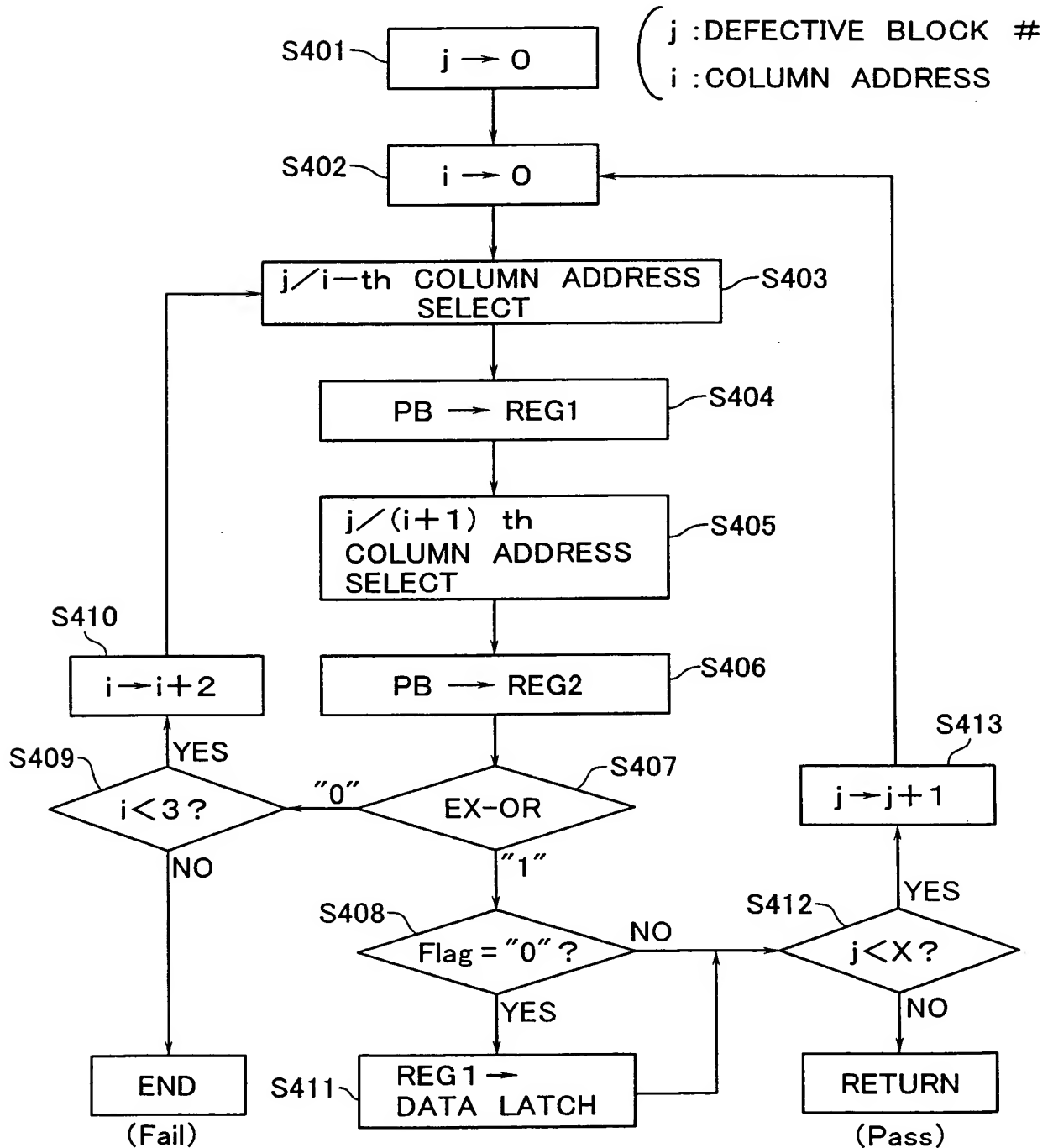
YES → S411 — REG1→ DATA LATCH

FIG.16

INITIAL SETUP DATA PROGRAMMING
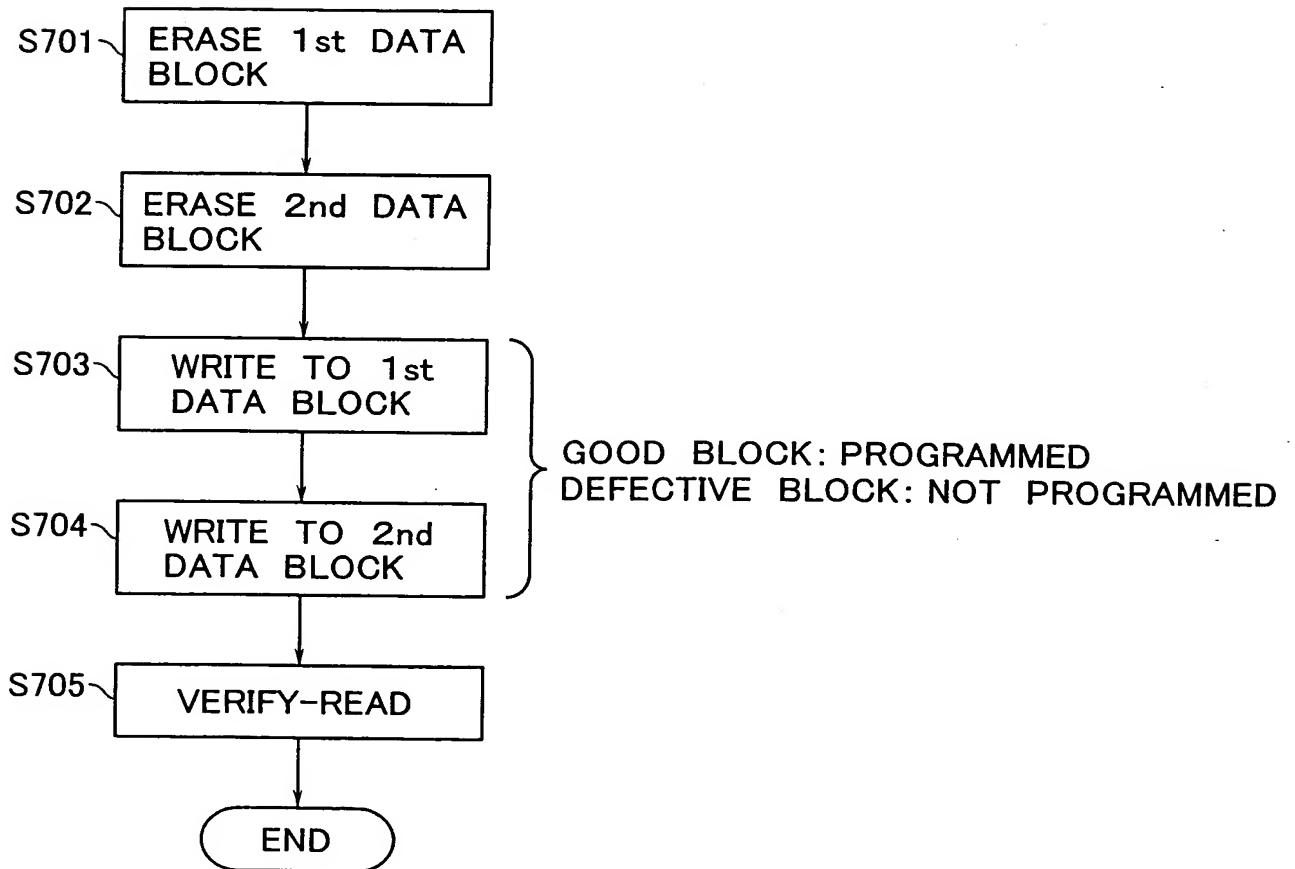(WITHOUT AUTOMATIC TEST)
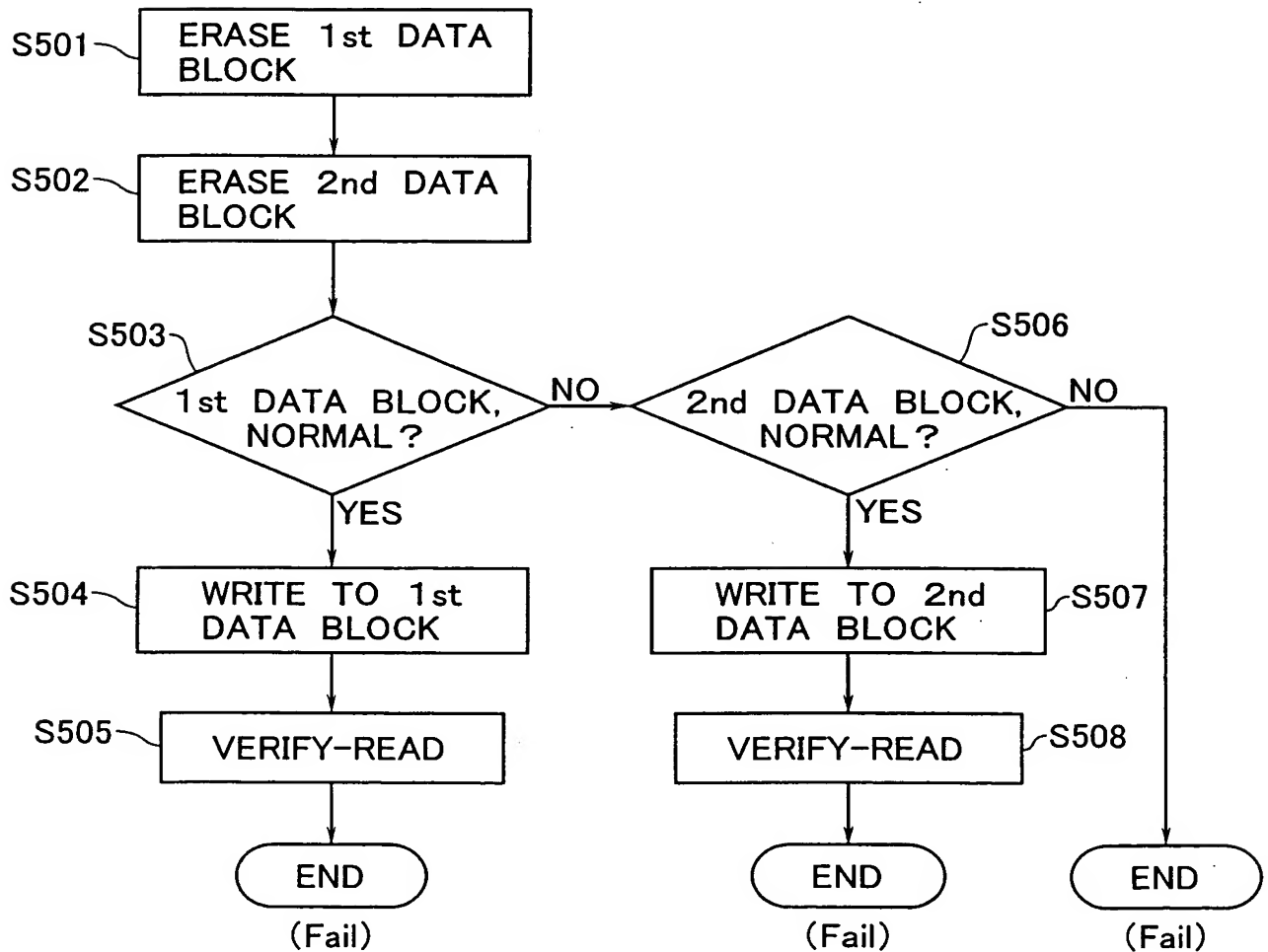
FIG.17

DATA BLOCK WRITE AT S504 & S507
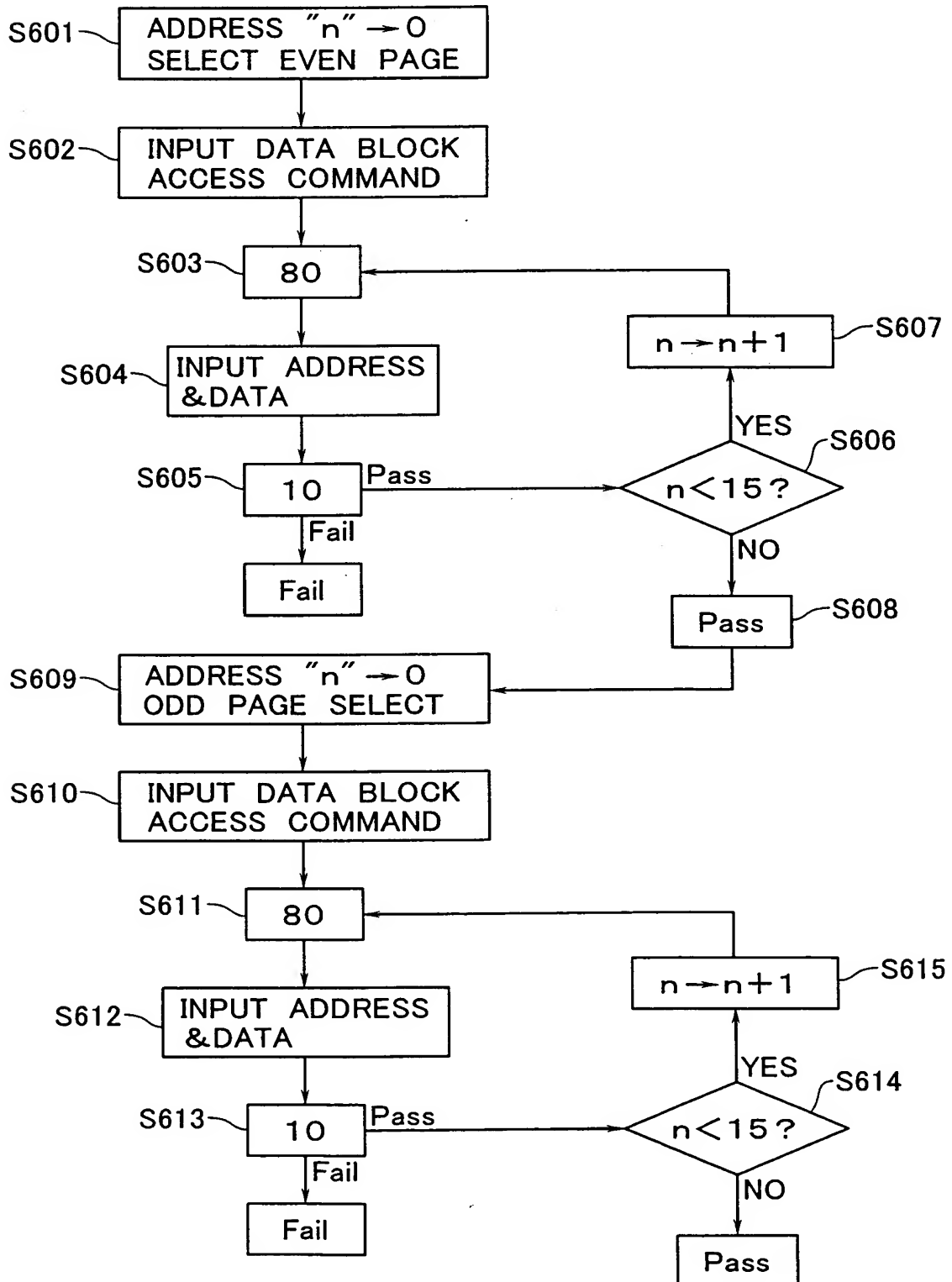
FIG.18

INITIAL SETUP DATA PROGRAMMING
(WITH AOTOMATIC TEST)

S701 — ERASE 1st DATA BLOCK

S702 — ERASE 2nd DATA BLOCK

S703 — WRITE TO 1st DATA BLOCK

S704 — WRITE TO 2nd DATA BLOCK

GOOD BLOCK: PROGRAMMED
DEFECTIVE BLOCK: NOT PROGRAMMED

S705 — VERIFY-READ

END

FIG.19

DATA BLOCK WRITING S703 & S704